An ARM Cortex-M0 Based FPGA Platform in Teaching Computer Architecture

Sang Don Kim and Seung Eun Lee*
Dept. of Electronic Engineering
Seoul National University of Science and Technology
Seoul, Korea
*Email: seung.lee [AT] seoultech.ac.kr

Abstract—**In this paper, we present an AMBA peripheral along with ARM Cortex-M0 processor on FPGA. The proposed platform provides the external interface signals to control the external IP based on AMBA interface. Moreover, µC/OS-II provides the way to control integrated hardware IPs. With our platform, students are visually able to validate the correctness of their IP along with ARM processor. The goal of the course is to effectively educate students with hand-on-experience, rather than designing a flawless IP. Our experience reveals that the proposed platform provides feasible way to AMBA based hardware IP verification.**

Keywords-Cortex-M0, AMBA, AHB-Lite, FPGA, uC/OS-II, Education

I. INTRODUCTION

A microprocessor has system bus to connect integrated IPs such as memory, I/O, and hardware accelerators. The system bus defines various signal set because the performance and the reliability are important in data communication. The Advanced Microcontroller Bus Architecture (AMBA) is an open-standard, on-chip interconnect specification for the microprocessor system. The AHB-Lite, which is a kind of AMBA signal set, allows one master unit on the system bus. It reduces the arbitration signals, and properly adopted in the low power processor system [1]. In order to implement the AHB-Lite peripherals, the signal set which is associated with read and write operation is required. AHB-Lite interface signals using the Xilinx FPGA was emulated [2] and a transaction level model of AMBA was presented [3]. AHB bus protocol checker focusing on efficient debugging mechanisms was proposed [4]. Recently, we had implemented the peripheral hardware using the AHB-Lite interface [5-6]. For teaching computer architecture, an incremental methodology with an FPGA system was proposed to complete the class project, designing a 5-stage pipelined 32-bit MIPS CPU [7].

In this paper, we propose a Cortex-M0 processor based FPGA platform for teaching computer architecture. The platform integrates an AMBA peripheral along with the processor, supporting external interface to control external IPs. Moreover, µC/OS-II provides the way to control integrated IPs. Using our platform, a computer architecture course effectively educates students with hand-on-experience, designing an IP, integrating the IP using AMBA interface, programming microprocessor to access the integrated IP.

II. SYSTEM ARCHITECTURE

A. *Coetex-M0 based FPGA Platform*

A common processor includes peripheral such as memory, I/O interfaces and hardware accelerators. In order to expand the

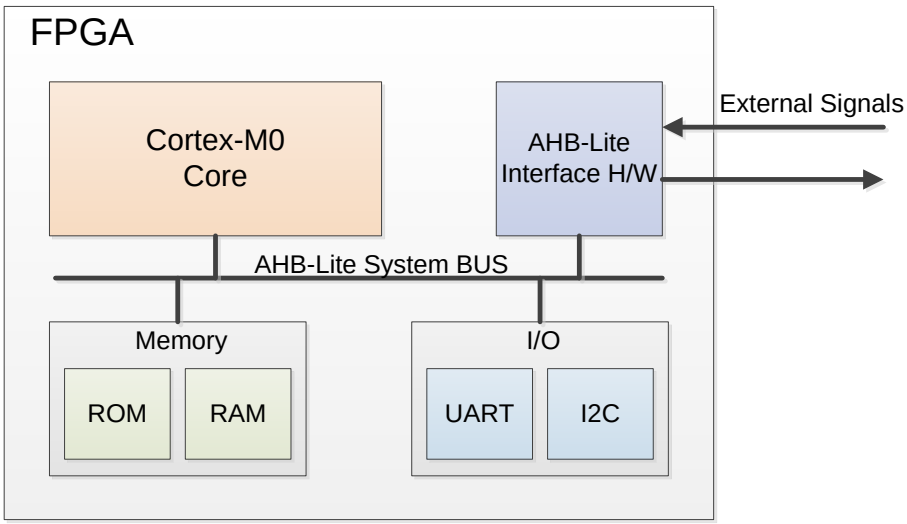

Figure 1. Block diagram of the Cortex-M0 based FPGA module

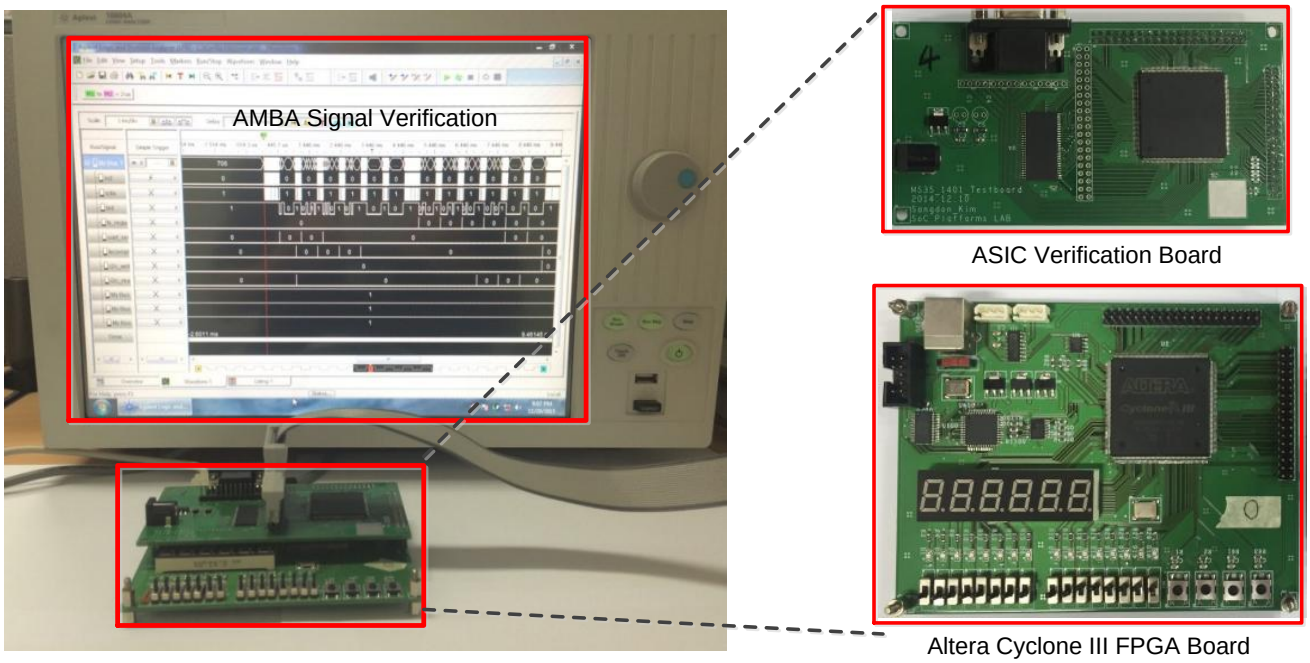

Figure 2. Environment for Hardware Verification

memory space, a processor supports the external memory interfaces. The proposed FPGA platform supports the external AHB-Lite bus interface associated with read and write operation. Figure 1 shows the block diagram of the proposed platform, which includes a Cortex-M0 core, an AHB-Lite system bus, a memory, an I/O and an AHB-Lite interface. In order the tailor the platform according to the physical constraints such as number of available pins, a student can easily change the bus width and address map of peripherals by modifying the RTL code. Our platform provides design template written in Verilog HDL for integrating the hardware IP into the platform.

B. AHB-Lite Interface Hardware

AHB-Lite interface hardware connects the external hardware IP and the AHB-Lite system bus. It supports many options to improve the connectivity of interfaces. It adjusts the clock speed of signals in order to compatible the FPGA I/O timing. Also, it has an option for the AMBA command translation. When this option is enabled, the AHB-Lite interface command is translated to the memory read/write command. If the external IP has asynchronous signal properties, the AMBA command translation is useful feature.

C. uC/OS-II Operating System

The Operating System provides easy way to manage the hardware. The uC/OS-II, which is real time based operating system, was ported on our platform. This operating system enables real time operation of the peripheral hardware. All of the peripheral hardware has to complete the read/write operation using the *HREADYOUT* signal; which is 1-bit data in the AHB-Lite interface. The timer interrupt of the operating system determines the status of hardware, and schedule the tasks. The real time property is important in the IoT hardware implementation.

III. IMPLEMENTATION

We adopt the Altera Cyclone III FPGA (EP3C25Q240) for implementation of the Cortex-M0 based FPGA module whose feature includes 148 I/O pins. The number of I/O pins is the primary constraint because of the AHB-Lite interface hardware requires dozens of data, address and command signals. Figure 2 shows our experimental environment which consists of the FPGA board and the ASIC SoC controlled by AHB-Lite interface. The FPGA board operates at 50MHz which is the main clock of the Cortex-M0 core. The SoC operating on the same frequency and it contains intra body communication hardware. As a result, the Cortex-M0 core, which is included in the FPGA module, controls the external SoC through the AHB-Lite interface hardware. In our experimental results, the Cortex-M0 core controls the external hardware IP, and timing of the signals is verified using a logic analyzer. Also, it provides a debug software property based on the uC/OS-II operating system. Therefore, the proposed FPGA module accelerates the design and the verification of hardware IP based on the AMBA bus interface.

IV. CONCLUSION

In this paper, we introduced the architecture of Cortex-M0 processor based FPGA platform for teaching computer architecture, which controls an external AMBA IP. µC/OS-II provides the way to control integrated IPs. We believe that a computer architecture course effectively educates students with hand-on-experience, designing an IP, integrating the IP using

AMBA interface, programming microprocessor to access the integrated IP, by using our platform. In the future, we plan to implement the advanced AMBA verification module based on the AXI bus. It will expand the usability of the proposed module.

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Direct questions and comments about this article to Seung Eun Lee, #202 Changhak Hall, 232 Gongreung-ro, Nowon-gu, Seoul, 139-743, KOREA; seung.lee@seoultech.ac.kr.

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